NISIN

触摸显示模组产品规格承认书

Displaly Module Specifications for Approval

客户： 客户型号：			NS598HD4001AZ01		
批准 APPROVED	审核 CHECKED	拟制 DESIGNED	批准 APPROVED	审核 CHECKED	拟制 DESIGNED

修改记录

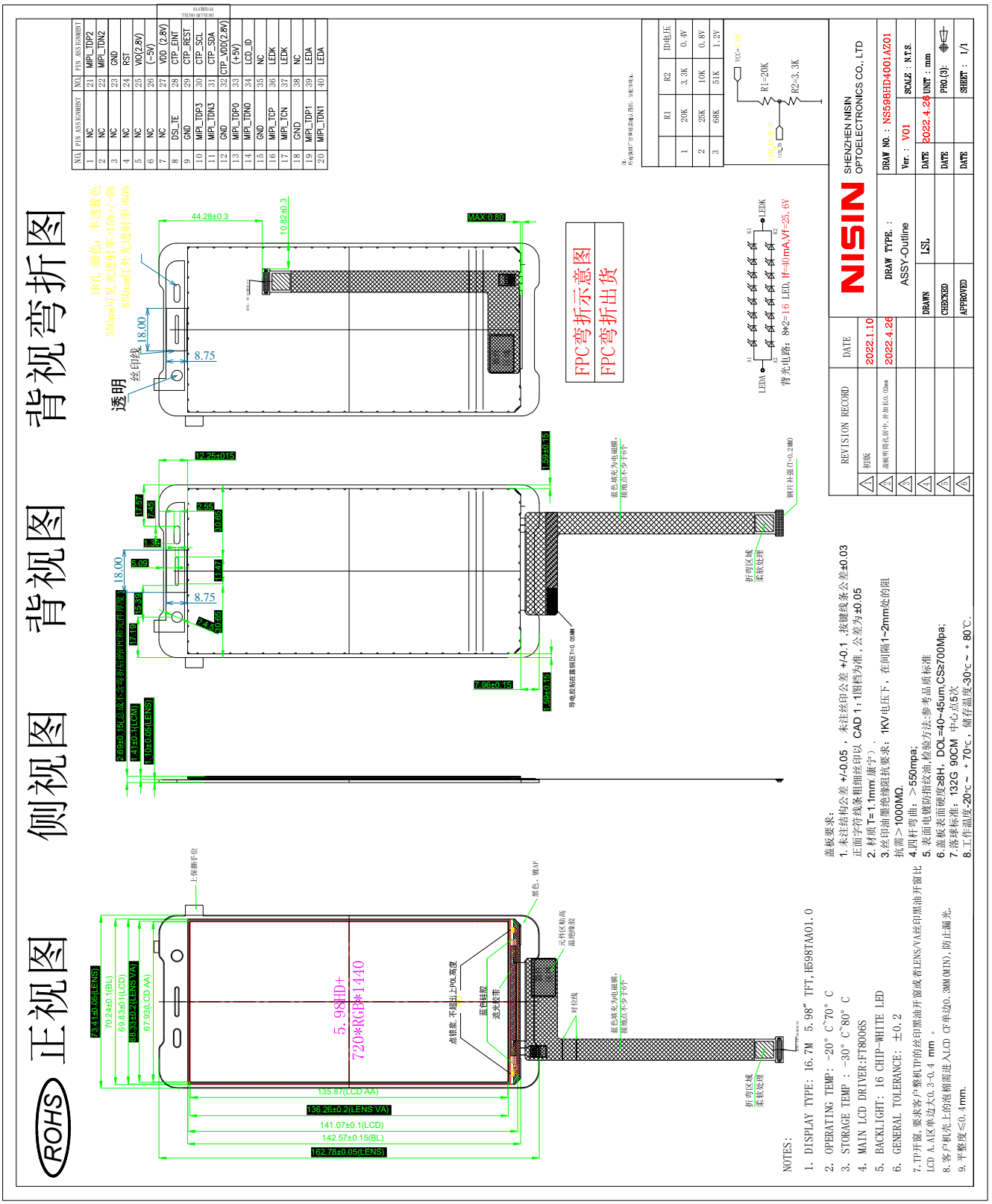
日期	版本	修改内容	页数	拟制
2022-5-12	V00	初版发行	所有	

目录

1.产品规格（Product Specifications）

面板类型（Panel Type）	In Cell TFT LCD
面板尺寸(Panel Size)	5.98 inch
显示类型（Display Type）	Normal Black
分辨率（Resolution）	720(RGB) x 1440 (dot)
显示点间距（Dot Pitch）	20.7Um X 60.1Um
显示色彩（color）	16.7M
视角（View Angle）	U/D/L/R: 80/80/80/80
显示驱动 IC（Display Driver IC）	FT8006S
接口类型（Interface Type）	MIPI 4 Lane
触摸类型（TP Type）	INCELL
触摸 IC （TP IC）	FT8006S
外形尺寸（Dimensions）	73.41(H) X 162.78(V) X 2.69(T)(mm)
显示区尺寸（Display area）	67.93 x 135.87(mm)
模组亮度（Module Brightness）	450Cd/m^2 （TYP）
触摸点数 Touch points	5
触摸按键 Touch Key Number	0
触摸屏固件版本	Version:

2.产品图纸（Product Drawings）



NO.	PIN ASSIGNMENT	NO.	PIN ASSIGNMENT
1	NC	21	MIPI_TDP2
2	NC	22	MIPI_TDN2
3	NC	23	GND
4	NC	24	RST
5	NC	25	VIO(2.8V)
6	NC	26	(-5V)
7	NC	27	VDD (2.8V)
8	DSI_TE	28	CTP_EINT
9	GND	29	CTP_REST
10	MIPI_TDP3	30	CTP_SCL
11	MIPI_TDN3	31	CTP_SDA
12	GND	32	CTP_VDD(2.8V)
13	MIPI_TDP0	33	(+5V)
14	MIPI_TDN0	34	LCD_ID
15	GND	35	NC
16	MIPI_TCP	36	LEDK
17	MIPI_TCN	37	LEDK
18	GND	38	NC
19	MIPI_TDP1	39	LEDA
20	MIPI_TDN1	40	LEDA

	R1	R2	ID电压
1	20K	3.3K	0.4V
2	25K	10K	0.8V
3	68K	51K	1.2V

3. 接口定义（The Interface Definition）

NO.	PIN ASSIGNMENT
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	DSI_TE
9	GND
10	MIPI_TDP3
11	MIPI_TDN3
12	GND
13	MIPI_TDP0
14	MIPI_TDN0
15	GND
16	MIPI_TCP
17	MIPI_TCN
18	GND
19	MIPI_TDP1
20	MIPI_TDN1

NO.	PIN ASSIGNMENT
21	MIPI_TDP2
22	MIPI_TDN2
23	GND
24	RST
25	VIO(2.8V)
26	(-5V)
27	VDD (2.8V)
28	CTP_EINT
29	CTP_REST
30	CTP_SCL
31	CTP_SDA
32	CTP_VDD(2.8V)
33	(+5V)
34	LCD_ID
35	NC
36	LEDK
37	LEDK
38	NC
39	LEDA
40	LEDA

4.电性特性（Electrical Characteristics）

4.1 ABSOLUTE MAXIMUM RATINGS

7. ELECTRICAL SPECIFICATION

7.1. Absolute Maximum Ratings

(AVDD = 4.5V ~ 6.5V, AVEE = -4.5V ~ -6.5V, VDDI = 1.65V ~ 1.95V, Ta = -30°C ~ 87°C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 2	VDDAM-VSS	-0.3 ~ +1.95	V	
Power Supply voltage 4	VDDI_TP-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 5	AVDD-VSS	-0.3 ~ +6.5	V	
Power Supply Voltage 6	VSS-AVEE	-0.3 ~ +6.5	V	
Power Supply Voltage 7	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V	
Operating Temperature	Topr	-30 ~ +70	°C	
Storage Temperature	Tstg	-55 ~ +110	°C	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

4.2 DC CHARACTERISTICS

4.2.1 DC Characteristics for Panel Driving

7.2.1. Basic DC characteristic

(AVDD = 4.5V~6.5V,AVEE = -4.5V~-6.5V,VDDI = 1.65V~1.95V, Ta = -30°C ~ 87°C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	AVDD	Operating Voltage	4.5	5.5	6.5	V	
Analog Operating voltage	AVEE	Operating Voltage	-6.5	-5.5	-4.5	V	
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	
Digital Operating voltage	VDD	Digital supply voltage	1.075	1.2	1.5	V	
Hissi interface Operating voltage	VDDAM	MIPI supply voltage	1.65	1.8	1.95	V	
Touch Operating voltage	VDDI_TP	Touch supply voltage	1.65	1.8	1.95	V	
Input / Output							
Logic High level input voltage	VIH	-	0.7*VDDI	-	VDDI	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*VDDI	V	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8*VDDI	-	VDDI	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2*VDDI	V	
Logic High level input current	IIH	Vin = VDDI or VDDAM	-	-	1	uA	
Logic Low level input current	IIL	Vin = VDDI or VDDAM	-1	-	-	uA	
VCOM Operation							
VCOMDC output voltage	VCOM	-	-2.4	-	1.2	V	
Source Driver							
Gamma positive reference voltage	VGMP	VGMP<AVDD-0.5V	2.85	-	6.0	V	
Gamma negative reference voltage	VGMN	VGMN>AVEE+0.5V	-6.0	-	-2.85	V	
Source output voltage	VSD	-	VGMN	-	VGMP	-	
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	30	mV	
		+4.2V>Sout>+0.8V	-	-	20	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	30	mV	
		-4.2V<Sout<-0.8V	-	-	20	mV	
Output offset voltage	V_{OFSET}	-	-	-	100	mv	
Reference Voltage							
Internal reference voltage	V_{REF}	-	1.94	2.0	2.06	V	
Internal reference voltage	V_{REF_TP}	-	2	3.5	4.5	V	

Booster operation							
Pump output voltage	VGH	Range=(AVDD-AVEE) ~(3XAVDD-2 AVEE)	5.5	-	18	V	
Pump output voltage	VGL	Range=(AVEE+AVEE) ~(2AVEE-AVDD)	-18.0	-	-5.5	V	
Regulator output voltage	VCL	-	-3	-3	-3.75	V	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

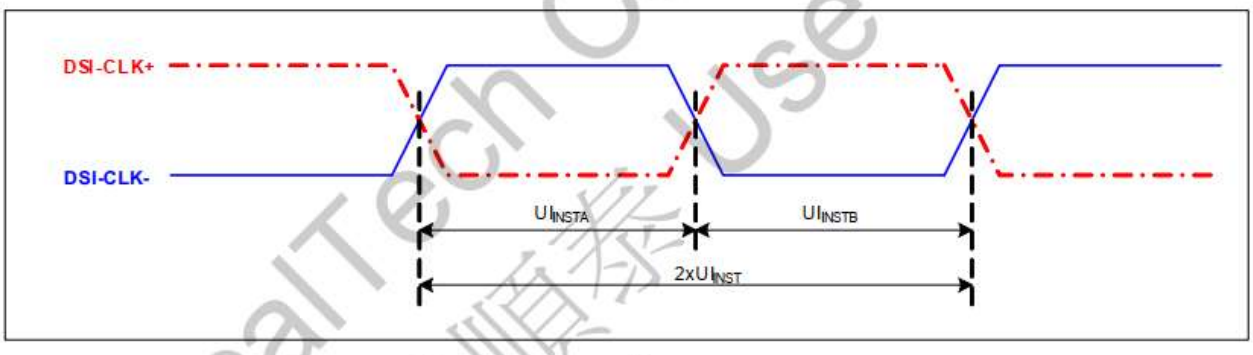
Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.1	1.2	1.3	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNDSH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	LVDSVDD	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	LVDSVDD	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedence	ZID	-	80	100	125	ohm

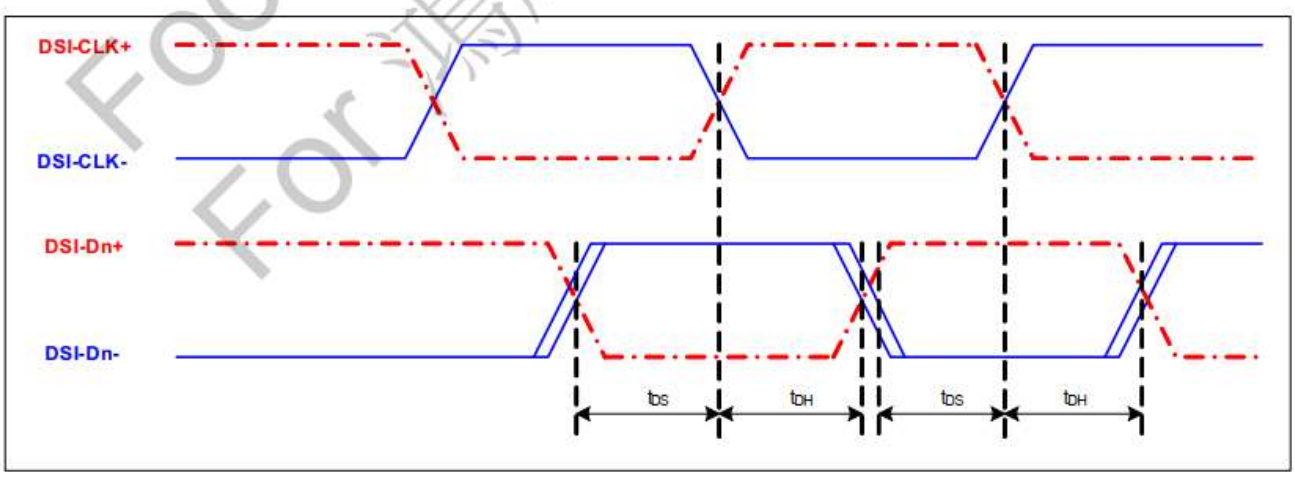
4.3 AC CHARACTERISTICS

7.3.2. MIPI-DSI characteristics

7.3.2.1. DPHY High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	1.67	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	0.84	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps





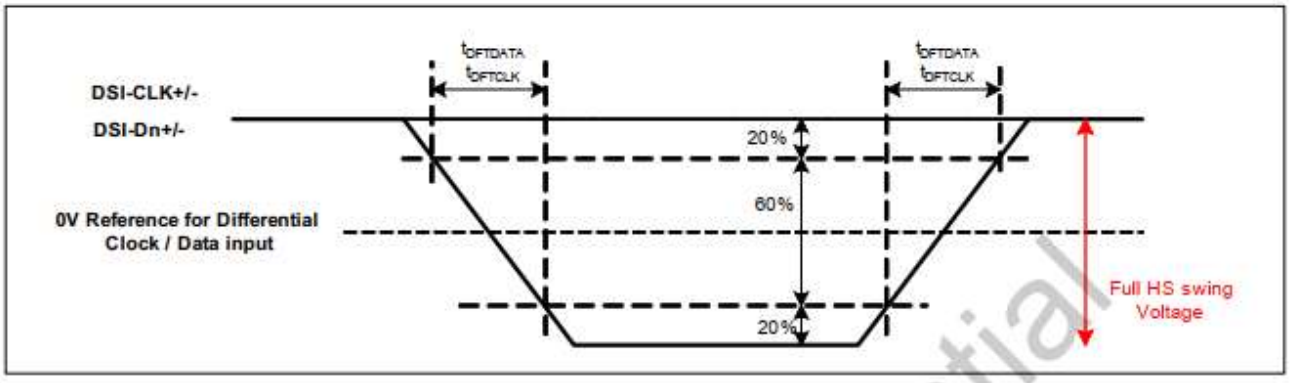


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.2.2. DPHY Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	-

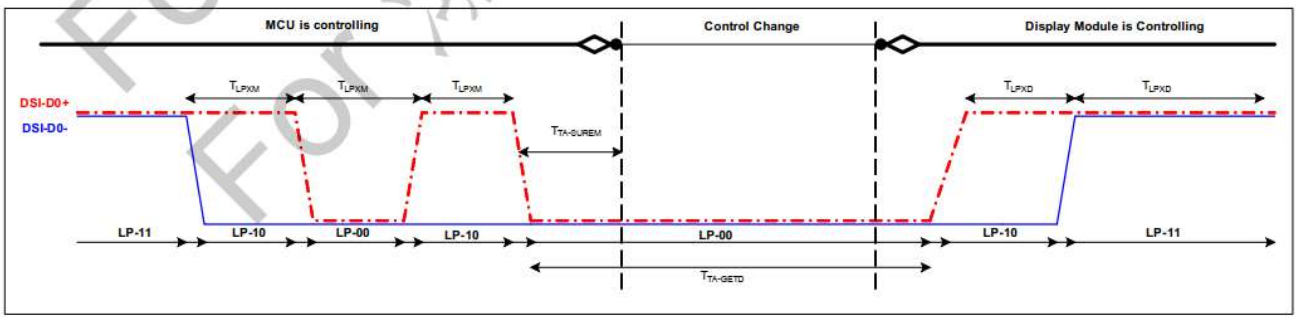


Figure: BTA from the MCU to the Display Module

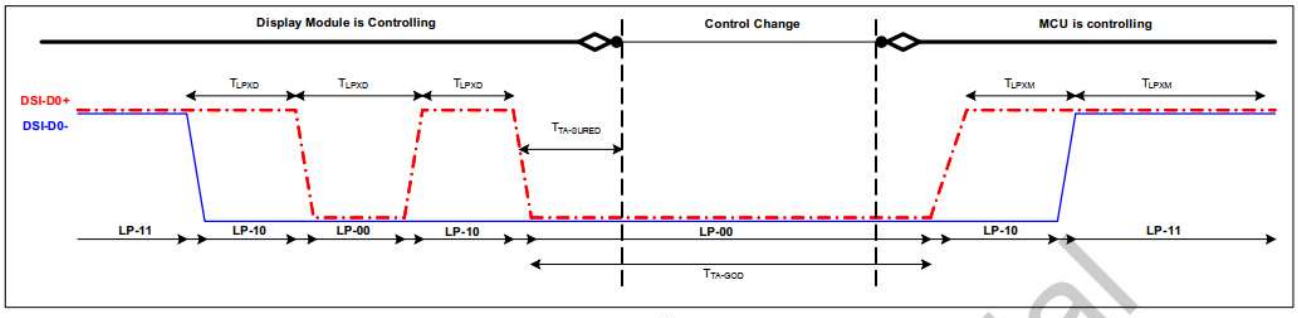


Figure: BTA from the Display Module to the MCU

7.3.2.3. DPHY Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

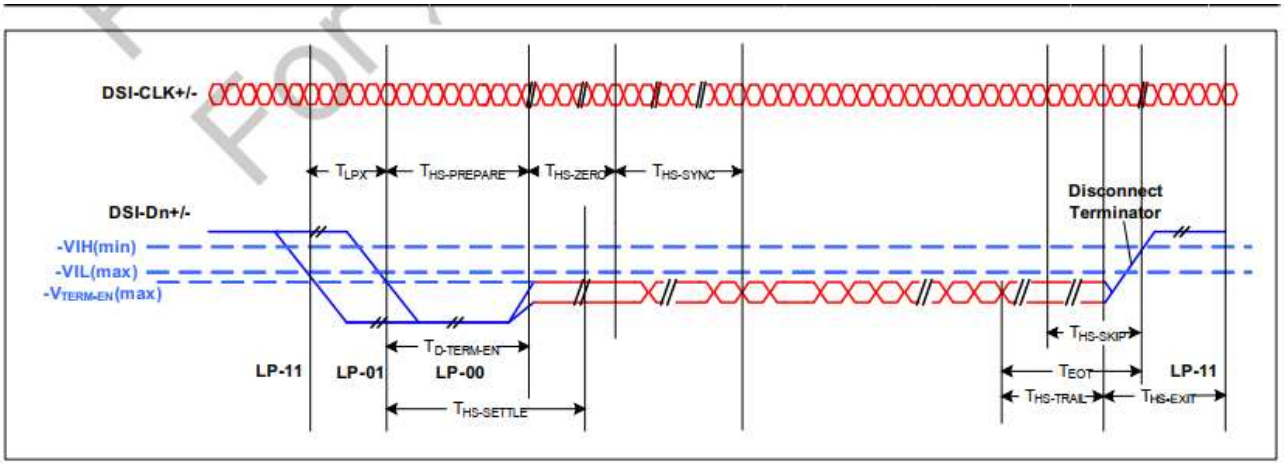


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

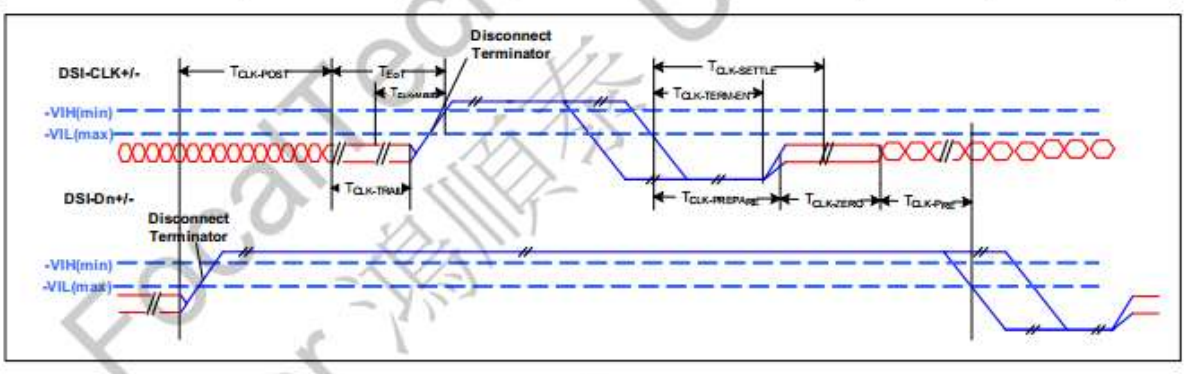
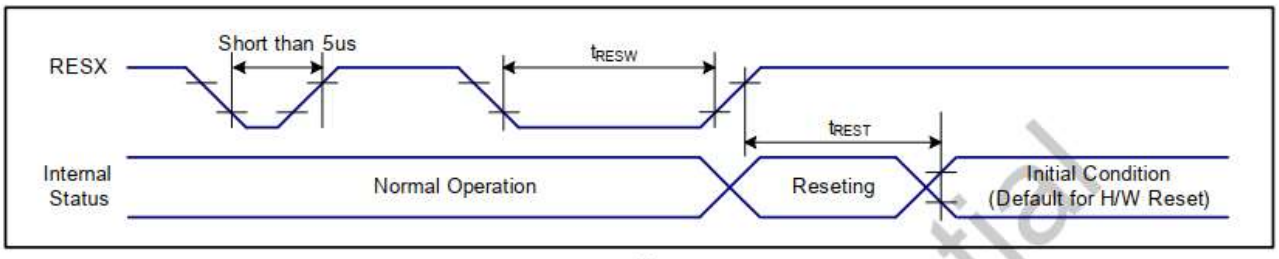


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.3. AC characteristic

7.3.1. Reset timing characteristics



VSS=0V, VDDI=1.65V to 3.6V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pin	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	Reset applied aduring Sleep-in mode	us
			70	-	-	Reset applied during Sleep-out mode	ms
t_{REST}	*2) Reset complete time	-	-	-	10	Reset applied during Sleep-in mode	ms
		-	-	-	120	Reset applied during Sleep-out mode	ms

Table: Reset input timing

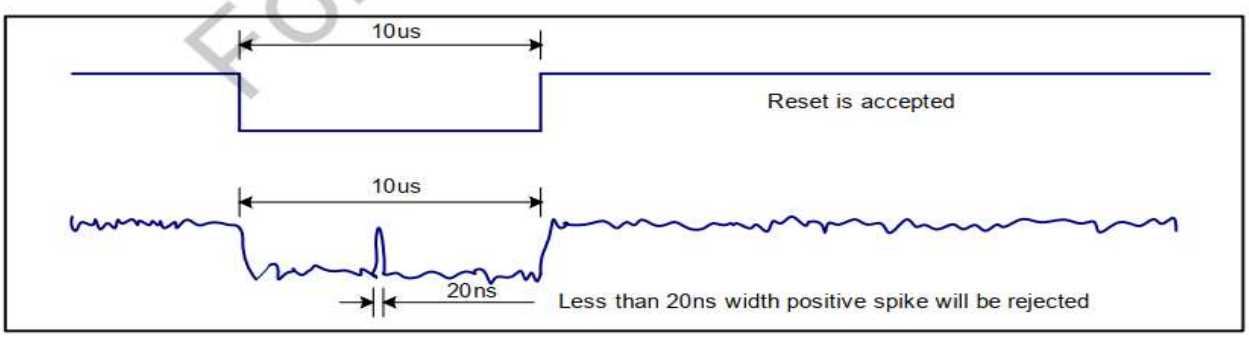
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset starts in Sleep-out mode. The display remains the blank state in Sleep-in mode) and then return to default condition for H/W reset.

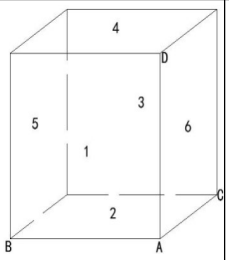
Note 3. During Reset complete time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 10ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 10msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

5.可靠性实验测试(Reliability Test Conditions And Methods)

<table>
<tr><th>序号</th><th>试 验项目</th><th>试验条件及方法</th><th>试验设备</th><th>检验项目</th><th>检验工具</th></tr>
<tr><td>1</td><td>高 温高 湿(静、动 态) 试验</td><td>温度 60℃±3℃,湿度 90%±3%,要求选择时间分别为 96 小时,静、动态（产品点亮）在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>恒温恒湿试验机</td><td>检验外观、功能、抗腐蚀性</td><td rowspan="2">目视/测试架/客户样机/显微镜</td></tr>
<tr><td>2</td><td>高 、低 温冲 击试验</td><td>静态-30℃（30 分钟）∽ 80℃（30 分钟）∽ -30℃（30 分钟），24 个循环，在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>冷热冲击试验机</td><td>检验外观、功能</td></tr>
<tr><td>3</td><td>高 温存 贮试验</td><td>常温70℃+-3℃、宽温80℃+/-3℃、96小时后在室温状态下恢复1 小时在2 小时内完成外观、显示功能检查。</td><td>烤箱</td><td>检验外观、功能</td><td rowspan="2">目视/测试架/客户样机</td></tr>
<tr><td>4</td><td>低 温存 贮试验</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃、条件的试验箱内保存96小时后在室温状态下恢复1 小时，在2 小时完成外观、显示功能检查，特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td></tr>
<tr><td>5</td><td>低温存贮试验（动态）</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃条件的试验箱内点亮刷屏，过程中每1小时观察一次，检查显示功能，如：异常，卡机，花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td><td>目视/测试架/客户样机</td></tr>
<tr><td>6</td><td>包 装模 组跌 落试验</td><td>1、跌落重量及自由落体高度:（图二）
 

2、自由落体角度如下：
<table><tr><th>总重量</th><th>自由落体高度</th></tr><tr><td>0-9kg</td><td>92cm</td></tr><tr><td>9-25kg</td><td>76cm</td></tr><tr><td>25-45kg</td><td>53cm</td></tr><tr><td>45-68kg</td><td>46cm</td></tr><tr><td>大于 68kg</td><td>41cm</td></tr><tr><td></td><td></td></tr></table>1） 一角：A角
2） 三菱：A-B,A-D,A-C
3） 六面：面 1,面 2,面 3,面 4,面 5，面 6;</td><td>包装模组跌落架</td><td>测试电性能无异常、外观检验无破损，无脱离现象</td><td>目视/测试架/客户样机</td></tr>
</table>

7	盐雾试验	标准条件:中性盐雾试验（NSS 试验）：5%的氯化钠盐水溶液,溶液 PH 值中性（6.5～7.2），试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间,时间 24h。2.其它特殊要求条件:醋酸盐雾试验(ASS 试验)：5%氯化钠溶液中配入冰醋酸,溶液 PH 值为 3 左右，试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间，时间 24h。	盐雾试验设备	检验外观、功能，盐雾试验结果的判定方法，腐蚀物出现判定法：定性判定，试验后功能测试应 OK,外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜
8	ESD 抗静电试验	测试架测试状态下试验：接触 4KV,非接触(空气）8KV 放电测试	抗静电枪（尖头接触放电，圆头空气放电）	检验外观、功能	目视/测试架

6. 光电参数（Optical Characteristics）

6.1 光学规格（Optical Specifications）

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time		Tr+Tf	θ=0° Φ=0°	--	25	35	ms	Note 3
		Tgray		--	35	40	ms	
Contrast ratio		CR	At optimized viewing	1000	1500	--	--	Note 4
NTSC		%	θ=0°	65	70	--	%	Measured by: CIE1931
Viewing Angle	Top		CR ≧10	75	80	--	deg.	Note 5
	Bottom					--		
	Left					--		
	Right					--		

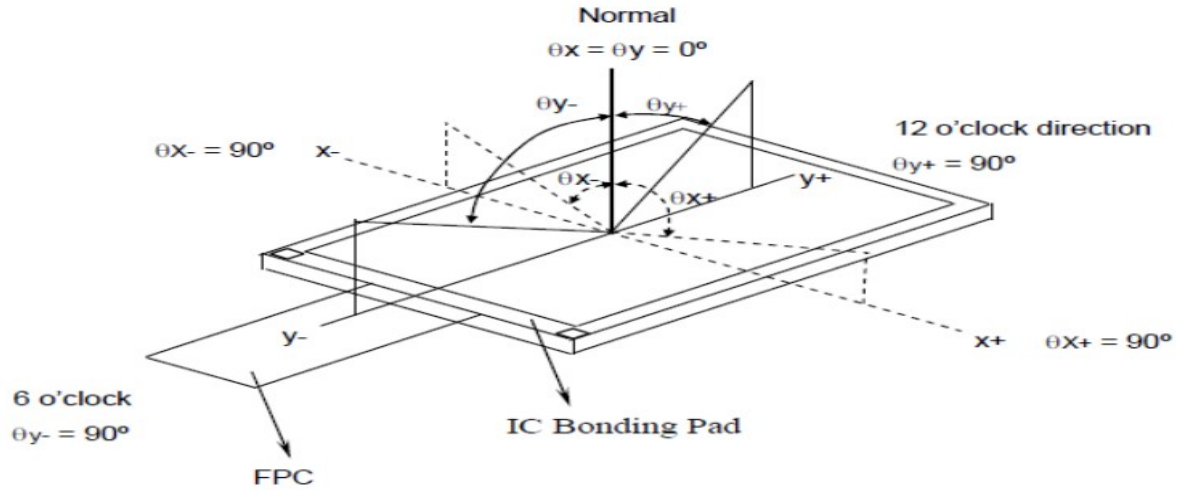
Transmittance		%	θ=0°		4.06		%	w/ APCF, w/ haze BLU: Silicate(聚飛) G50
Crosstalk	%	25℃		--		2	%	Note 7
Gamma				1.9	2.2	2.5		
Chromaticity	White	X	θ=0°	0.274	0.294	0.314		1. LED使用Silicate(聚飛) G50 2. Without PEDOT(未镀膜)
		Y	θ=0°	0.304	0.324	0.344		
	Red	X	θ=0°	0.614	0.634	0.654		
		Y	θ=0°	0.309	0.329	0.349		
	Green	X	θ=0°	0.291	0.311	0.331		
		Y	θ=0°	0.583	0.603	0.623		
	Blue	X	θ=0°	0.131	0.151	0.171		
		Y	θ=0°	0.029	0.049	0.069		

Note 1: Measured under Ambient temperature =25℃±2℃ in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1° by luminance meter, after 15 minutes operation.

6.2 视角定义（Description of View Angle）

Measurement Set Up



7.检验标准（Inspection standard）

9.1 Inspection conditions is as follows

1) Viewing angle is within +-30° from vertical direction, as fig 1

2) Viewing angle is the angle defined in the drawing

3) Ambient temperature is approximately 25+-5° C

4) Ambient luminance is about 300~500 Lux.

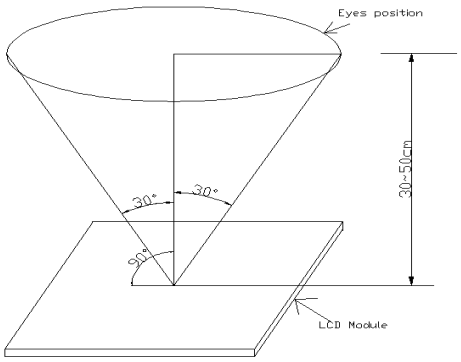
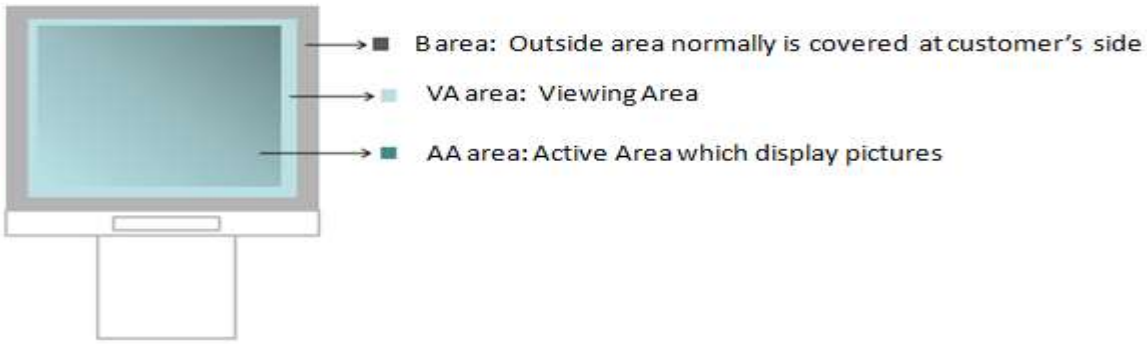


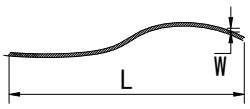
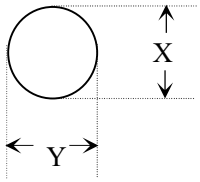
fig1

9.2 Panel area definition



9.3 Routine inspection standards

项目	不良定义	不良现象	判定标准			检验方法	
9.3.1	外观尺寸	与图纸尺寸不相符	NG			卡尺	
9.3.2	功能	显示少线	NG			目视	
		无显示	NG			目视	
		显示异常	NG			目视	主
		TP 功能不良，无触摸	NG			目视/用手触摸	主
9.3.3	*点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的点状物*	*偏光片刺伤、脏点、圆形物、黑点* *Φ=(L+W)/2*	LCM/总成 0.95 寸—2.4 寸			目 视 (用菲淋卡比对)	次
			Φ≦0.10mm		1、距产品 30mm 目视不见忽略。2、5mm 间距内只允许 3 个点。3、显示区只允许 10 个点，超过以上第 2 第 3 项则 NG 。		
			0.10mm<Φ≦0.15mm		1		
			Φ>0.15mm		NG		
			0.15mm<Φ≦0.2mm 按照 A-品入库				
			LCM/总成>2.4 寸——6.0 寸			目 视 (用菲淋卡比对)	
			Φ≦0.10mm		1、10mm 间距内只允许 3		

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td>个
2、显示区只允许 10 个点，超过以上任意一项则 NG</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>0.1mm＜Φ≤0.15mm</td><td></td><td>4（TP、屏各允许 2 个）</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>0.15mm＜Φ≤0.2mm</td><td></td><td>2（TP、屏各允许 1 个）</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>Φ>0.2mm</td><td></td><td>NG</td><td></td><td></td></tr>
<tr><td>9.3.4</td><td>点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的线状物/刮伤</td><td>  </td><td colspan="3">LCM/总成 0.95 寸——6.0 寸
<table><tr><td></td><td></td><td rowspan="2">允许个数</td></tr><tr><td>长(L)</td><td>宽(W)</td></tr><tr><td>≦1mm</td><td>≦0.03mm</td><td>2</td></tr><tr><td>≦2mm</td><td>0.03<W≦0.05mm</td><td>1</td></tr><tr><td>>2mm</td><td>>0.05mm</td><td>NG</td></tr></table>两条线毛之间必须距离 5mm 以上（0.95 寸—3.0 寸）.
两条线毛之间必须距离 10mm 以上（3.1 寸—6.0 寸）.</td><td>目视(用菲淋卡比对)</td><td>次</td></tr>
<tr><td>9.3.5</td><td>偏光片气泡</td><td>Φ=（X+Y）/2
  </td><td colspan="3"><table><tr><td>尺寸</td><td>允许个数</td></tr><tr><td>1、Φ≦0.1mm
2、不超过边框 1/3</td><td>不计(密集不可)</td></tr><tr><td>0.10＜Φ≦0.2mm</td><td>1</td></tr><tr><td>Φ＞0.2mm</td><td>NG</td></tr><tr><td>0.2＜Φ≦1.5mm,（边框以外）</td><td>3</td></tr></table>0.95 寸-2.4 寸气泡间距大于 5mm 以上
>2.4 寸-6.0 寸气泡间距大于 10mm 以上</td><td>在日光台灯下撕起保护膜,距待测物 30cm 目视</td><td>次</td></tr>
<tr><td>9.3.6</td><td>T/P 及偏光片凹凸点</td><td>T/P:LCD 偏光片上有凹凸点</td><td colspan="3">可视区有水纹（擦拭不掉）拒收
未进入可视区允收,客户装机后不见允收</td><td>在同一视角下用样品比对</td><td>次</td></tr>
<tr><td>9.3.7</td><td>Mura</td><td>边框四周或任一侧的色差、较画面深、区域云状</td><td colspan="3">1.判定示画面为 128 灰阶画面，用 ND filter 盖住 mura 位置进行</td><td>ND filter,128 灰阶</td><td>次</td></tr>
</table>

		不均、固定位置之图形凹陷状、封口部分较画面深的半圆形、一圈圈均匀的色差、线状 mura、黑画面可见因 spacer 聚集产生的 mura、均匀的实斜线、区域性斜线、Driver IC 与 TFT 匹配问题等原因的 mura	判定。 2、ND1.3（ND5%可遮盖不见） 3、双方若有签 限度样品，优先限度样品。	画面	

8.模组使用注意事项（Precautions for Use of LCD Modules）

8.1 如果接口定义内有定义 IM0，请根据规格书（4.接口定义）内的定义做正确选择以匹配数据线的位数。

8.2 客户在做结构设计时，请保证机壳开窗尺寸比触摸屏 V.A 单边少 0.3mm。泡棉开窗尺寸比触摸屏 V.A 单边大 0.2mm。

8.3 模组的主要部件 LCD 和 TP 都是由玻璃组成，在测试、使用、移动过程中，请轻拿轻放。当产品不带触摸屏时，靠近 FPC 的屏幕两端绝对不能受力，否则会导致玻璃破损和显示不良的发生。

8.4 粘合偏光片、背光、触摸屏的胶材是有机物质，在接触到甲苯、乙醇、丙酮时，会破坏粘性。在使用中，请防止这些物质接触到产品。

8.5 如果显示表面掉落有灰尘、异物，切忌用手直接擦拭。请用棉签轻轻挑擦。

8.6 如果 LCD 破损导致液晶泄露，请不要让皮肤或衣服沾到液晶。如果不小心碰到，请立即用肥皂和清水清洗。

8.7 用手直接触摸显示区域会造成偏光片的损坏，同时容易引起静电问题。

8.8 当模组运行时，在显示区域施加压力会导致显示不正常。撤去外力，重新开机，可以恢复。

8.9 潮湿的坏境可能引起玻璃 ITO 的腐蚀，在使用中，请确保湿度在 50%一下。